Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A solid-state imaging device, comprising:

a pixel array having a plurality of unit pixels, each of the unit pixels including a photo diode and an insulated gate field effect transistor that detects photocharges; and

a control circuit that controls the operation of the pixel array, wherein:

the photo diode and the insulated gate field effect transistor share a well region of a first conductivity type that is formed in a semiconductor layer of a second conductivity type, the semiconductor layer of the second conductivity type being formed on a semiconductor substrate of the first conductivity type;

an accumulation region that accumulates charges of a given conductivity type generated in response to light incident on the photo diode that is formed in the well region of the insulated gate field effect transistor; and

the control circuit configured to forward ~~biases~~bias a junction region between the semiconductor substrate and the semiconductor layer so as to accumulate a predetermined amount of the charges of the given conductivity type during pre-charging regardless of an amount of the charges of the given conductivity type before pre-charging in the accumulation region, and discharges the charges of the given conductivity type accumulated in the accumulation region thereafter.

2. (Original) The solid-state imaging device according to claim 1, the insulated gate field effect transistor further comprising:

a source diffused region of the second conductivity type formed on a surface of the well region;

a drain diffused region of the second conductivity type formed on a surface of the semiconductor layer other than the surface of the well region;

a gate electrode formed above the well region between the drain diffused region and the source diffused region with a gate insulating film therebetween;

a channel region formed in the surface of the well region below the gate electrode and having an impurity layer of the second conductivity type; and

the accumulation region being a heavily doped buried layer of the first conductivity type formed below the channel region in the well region and adjacent to the

source diffused region, having an impurity concentration higher than that of the well region; and

the control circuit applies predetermined voltage to at least the drain diffused region to forward bias the junction region so as to accumulate a predetermined amount of the charges of the given conductivity type in the accumulation region, and discharges the charges of the given conductivity type accumulated in the accumulation region thereafter.

3. (Original) The solid-state imaging device according to claim 1, wherein a state where a predetermined amount of the charges of the given conductivity type are accumulated is a saturated state where a maximum amount of available charges of a given conductivity type are accumulated in the accumulation region.

4. (Original) The solid-state imaging device according to claim 1, the charges of the given conductivity type being holes if the first conductivity type is a P type and the second conductivity type is an N type.

5. (Original) The solid-state imaging device according to claim 1, the charges of the given conductivity type being electrons if the first conductivity type is an N type and the second conductivity type is a P type.